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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,568	02/25/2002	Stephen M. Gates	YOR919980324 US2	9141

21254 7590 12/15/2004

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,568	GATES ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18,26-31 and 33-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-18,26-31 and 33-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 11-12, 18, 26, 28, 33, 36, 38-41 and 43 rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al (US. 5,895,947).

Regarding claims 11-12, 18, 26, 28, 33, 38, 40 and 43, Lee (Fig. 8) discloses an Array of microelectronic elements comprising: a substrate 100 of semiconductor material (column 4, lines 54-56); a lower layer 110/120/130/134 of dielectric material disposed with a lower surface in contact with the substrate 100 and an upper surface in spaced adjacent thereto; a pattern of mutually electrically isolated conducting regions disposed within the lower layer 110/120/130/134 of dielectric material (column 5, lines 22-36), the conducting regions extending to the upper surface of the lower layer; an

upper layer of dielectric material 30 (not shown in Fig. 8, see Fig. 1 and column 6, lines 10-18) disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer; and a plurality of capacitor nodes 142 made of polysilicon semiconductor material (column 5, lines 58-63) disposed within the upper layer of dielectric material 30 (also see Fig. 1), each of the nodes 142 being in electrical contact with only one of the conducting regions at the upper surface of the lower layer, wherein each conducting region comprises: a metal conductor (not labeled, see a first level interconnect wiring layer formed in a dielectric film 110 and column 2, lines 3-5); and a via e1 (not labeled in Fig. 8, see Fig. 6) which is filled with a TiN or W material (column 5, lines 22-30), the TiN or W material e1 extending between the metal conductor and a node 142 in the plurality of nodes and electrically connecting the metal conductor with the node 142 of capacitor semiconductor device. It is noted that the via filed with TiN or W material of Lee would inherently function as diffusion barrier because it is filed with the same diffusion barrier material as claimed (i.e., TiN, W).

Regarding claim 36, Lee (Fig. 8) further discloses a bonding promoting layer 134 formed on the lower layer of dielectric material, the bonding promoting layer 134 bonding the lower surface of the upper layer 30 of dielectric material to the upper surface of the lower layer 110/120/130.

Regarding claims 39 and 41, Lee (Fig. 8) further discloses that the via e1 comprises an area which is less than an area of the metal conductor, and the node 142 which is electrically connected to the metal conductor is aligned with the via e1 and the metal conductor.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11-12, 15-16, 18, 26, 28-29, 33-35, and 36-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al (US. 5,940,319) in view of Lee et al (US. 5,895,947).

With respect to claims 11-12, 18, 26, 28-29, 33, 35, 38, and 40-43, Durlam's first embodiment (Figs. 5-8) discloses an array of microelectronic elements comprising: a substrate of semiconductor material 11; a lower layer of dielectric material (12a,21,25) disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto; a pattern of mutually electrically isolated conducting regions (19a,37) and (19b,38) (Fig. 5) disposed within the lower layer of dielectric material, the conducting regions extending to the upper surface of the lower layer, an upper layer of dielectric material 51 disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer; and a plurality of nodes (43,45) and (44,46) comprising MTJs 43 and 44 and disposed within the upper layer of dielectric material, each of the nodes being in electrical contact with only one of the conducting regions at the upper surface of the lower layer, wherein each conducting region comprises: a metal conductor 19a and a via 37 formed on the metal conductor 19a, the via 37

extending between the metal conductor 19a and a node in the plurality of nodes and electrically connecting the metal conductor 19a with the node.

Durlam's first embodiment does not disclose the plurality of nodes including semiconductor diodes. However, Durlam further teaches a second embodiment of MRAM (Fig. 17) having a plurality of nodes, which include diodes 93 and 95 in contact with the conducting regions 82 at the upper surface of the lower layer. Accordingly, it would have been obvious to modify the first embodiment by forming the plurality of nodes with the structure as suggested by the second embodiment for the purpose of switching a magnetic memory element to read information in the magnetic memory element (column 6, lines 26-30).

Neither Durlam's first embodiment nor Durlam's second embodiment discloses the via is filed with the refractory diffusion barrier material. However, Lee (Fig. 8) teaches the forming of a plurality of conducting regions, each conducting region comprises: a metal conductor and a via e1 (see Fig. 6) which is filled with a diffusion barrier material of TiN or W (column 5, lines 22-30), the diffusion barrier material e1 contacting capacitor semiconductor node 142 of polysilicon (column 5, lines 58-63) and extending between the metal conductor and the node 142. Accordingly, it would have been obvious to further modify Durlam's device by filling the via 37 with the refractory diffusion barrier material because as taught by Lee, such material would provide excellent filling properties (column 5, lines 25-27) and would reduce the contact resistance between the via and the semiconductor node (column 6, lines 33-41).

With respect to claim 16, Durlam (Fig. 8) further discloses that the device comprises a field effect transistor 12a, a first insulating layer 54 is disposed over an upper surface of the upper layer, and a second insulating layer 33 is formed over the upper surface of the lower layer.

Regarding claim 15, it would have been obvious to form the semiconductor node of Durlam as a field effect transistor because it is an intended use depending upon the application, which is desired for the semiconductor node of Durlam.

Regarding claim 34, Durlam (Fig. 8) also discloses that each of the conductive region further comprises a metal layer 31 (or 24) in electrical contact with the via, the metal layer 31 (or 24) being formed of nickel-iron (column 3, lines 28-30) which is different than the aluminum/copper material of the via 37.

Regarding claims 36-37, Durlam's Fig. 7 further discloses a bonding promoting layer 33 of dielectric material formed on the lower layer 25 of dielectric material, the bonding promoting layer 33 bonding the lower surface of the upper layer 51 of dielectric material to the upper surface of the lower layer 33. As taught by Durlam, the bonding promoting layer 33 is placed between the lower layer 25 and the upper layer 51 to provide electrical isolation between the conductor layers (column 3, lines 60-64). Therefore, it would have been obvious to form the dielectric layer 33 as a glass layer because the glass layer would also provide the electrical isolation between the conductor layers. It is noted that the process limitation (softening temperature in a range of 400 degrees C to 500 degrees c) would not carry patentable weight in a claim

drawn to structure because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 39, Lee (Fig. 8) also teaches the via e1 comprising an area which is less than an area of the metal conductor formed below.

5. Claims 13-14, 17, 27, and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durlam et al and Lee et al as applied to claims 11 and 26 above, and further in view of Bronner et al (US. 6,242,770).

Durlam does not disclose that diodes are single crystal Si diodes.

However, it would have been obvious to form Durlam's diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes (column 9, lines 63-65) would provide high conductivity, high rectification and low total resistance (column 3, lines 1-4).

Response to Arguments

6. In the amendment filed 9/30/04, the scopes of base claims are changed and narrower by deleting "comprising" and inserting "which is filled with". Therefore, the new ground of rejection is applied.

Applicant argues that "Durlam clearly does not teach or suggest the importance of forming a diffusion barrier between a metal conductor and a semiconductor node," as amended.

This argument is not persuasive because the new reference issued to Lee et al (US. 5,895,947) clearly teaches the obviousness of forming a conducting region comprising: a via e1 filled with a diffusion barrier material and disposed between a metal

conductor and a semiconductor node 142 of polysilicon (see Fig. 8). The via filled with the diffusion barrier material would provide excellent filling properties (column 5, lines 25-27) and reducing the contact resistance between the via and the semiconductor node (column 6, lines 33-41).

Applicant asserts that Applicant surprises because the examiner relies on the teaching disclosed in figure 5 and the teaching disclosed in figure 17 of Durlam for the combination. According to Applicant, the embodiment "disclosed in Figure 17 of Durlam which is completely unrelated to the embodiment in Figure 5 of Durlam."

The examiner recognizes that one skilled in the art would not be surprised by the combination between these two embodiments because they are completely related to magnetic random access memory structure (MRAM), and because the motivation for the combination of these embodiments is clearly suggested (see ground of rejection for details).

Applicant also argues that it would not be obvious to combine Bronner with the applied references because Bronner does not teach or suggest a via formed on the metal conductor, and filled with a diffusion barrier as amended.

This argument is not persuasive because the new reference issued to Lee et al clearly suggests a via formed on the metal conductor and filled with a diffusion barrier material. Bronner is only relied on for showing that it was known to form a diode as a single crystal Si diode for providing high conductivity, high rectification and low total resistance (column 3, lines 1-4).

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
December 10, 2004

PHAT X. CAO
PRIMARY EXAMINER